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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,054	10/12/2001	Eishi Matsuda	KN-65-US	1008
466	7590	01/27/2004	EXAMINER	
YOUNG & THOMPSON 745 SOUTH 23RD STREET 2ND FLOOR ARLINGTON, VA 22202			CUNNINGHAM, TERRY D	
			ART UNIT	PAPER NUMBER
			2816	

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
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EXAMINER

ART UNIT	PAPER
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Commissioner for Patents

The information disclosure statement filed 12 September 2003 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because such does not include the certification under 37 C.F.R. § 1.97(e). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 C(1).

Terry D. Cunningham
Primary Examiner
Art Unit: 2816



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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 9

Application Number: 09/975,054
Filing Date: October 12, 2001
Appellant(s): MATSUDA, EISHI

Roland E. Long Jr.
For Appellant

EXAMINER'S ANSWER

MAILED
JAN 27 2004
GROUP 2800

This is in response to the appeal brief filed 14 November 2003.

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(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is correct.

However, Examiner has reconsidered the outstanding enablement and critical feature rejections under 35 U.S.C. § 112, first paragraph. While it may not be clear as to whether the specificity of the specification allows the invention to be made "without undue experience", there is insufficient evidence of the record to establish otherwise. Thus, the rejections to claims 1-10 under 35 U.S.C. § 112, first paragraph, are hereby removed.

The remaining issue is whether claims 1-10 are anticipated by Doluca et al. 4,769,784.

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(7) Grouping of Claims

The appellant's statement in the brief that certain claims do not stand or fall together is not agreed with because, with regard to the remaining anticipation rejection, it is not seen that the claim groupings are argued separately.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

4,769,784

Doluca et al.

9-199

(10) Grounds of Rejection

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Doluca et al. (USPN 4,769,784).

With respect to claims 1-3, Doluca et al. discloses, in Figs. 2-3, 5 and 6, a circuit comprising: “a DC power supply (V_{CC})”; “a DC-DC converter circuit (29, shown in Figs. 3 and 6)”; “a control signal (V_{PEN})”; “a first differentiating circuit (39 and 43, shown in Fig 5)”; “a current absorbing circuit (45, shown in Fig. 5)”; and “an output (19)”, all connected and operating similarly as recited by Applicant.

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With respect to claims 4-6, Doluca et al. discloses, in Figs. 2-3, 5 and 6, a circuit comprising: “a DC power supply (V_{CC})”; “a DC-DC converter circuit (27, shown in Fig. 5)”; “a control signal (output of 43)”; “a second differentiating circuit (31 and 35)”; “a current injecting circuit (37, shown in Fig. 3)”; and “an output (19)”, all connected and operating similarly as recited by Applicant.

Doluca et al. discloses, in Figs. 2-3, 5 and 7, a circuit comprising: “a DC power supply (voltage on CPL)”; “a DC-DC converter circuit (one of the capacitors corresponding to CPL (capacitor-plate line))”; “a first differentiating circuit (39 and 43)”; “a current absorbing circuit (45)”; “a second differentiating circuit (31 and 35)”; and “a current injecting circuit (37)”, all connected and operating similarly as recited by Applicant.

(11) *Response to Argument*

In the paragraph linking pages 16-17, Appellant discusses invention to Doluca et al. and in particular the “capacitor-plate line”. Then in the first three full paragraphs of page 17 goes on to argue “the DOLUCA circuit does not convert an inputted DC power supply voltage into a predetermined DC voltage, i.e., there is no conversion of DC supply voltage to a predetermined DC voltage at line 19 of Figure 2”. Examiner initially points out that these remarks are only discussing the rejection to claim 7. However, the rejection to claims 1-6 does not rely on the “capacitor-plate line” being the “DC-DC converter”. The rejection claims 1-6 are rely on either 27 or 29 of Fig. 2 as being the “DC-DC converter”. It is clear in the reference that elements 27 and 29 each convert “a predetermined DC power supply voltage (V_{CC}) into a predetermined DC voltage supply to the output (19)”. With respect to claims 7-10, the rejection is relying on a capacitor connected to plate line 19 as the DC-DC converter. Examiner contends that a

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capacitor, connected as disclosed by Doluca et al. will convert “a predetermined DC power supply voltage (at the input plate 19) into a predetermined DC voltage supply to the output (at the same point)”. Although a capacitor with such a connection is understood by one skilled in the art has the input and output commonly at the plate line, such would still be seen to read on the claim language since the claims do not recite that the DC power supply voltage is inputted distinctly from the output.

In the first paragraph of page 18, Appellant argues that a “charge pump...can not anticipate the DC-DC converter circuit recitation”. This statement is not at all understood. The phrase “DC-DC converter” is often used to refer to a “charge pump”. This is due to the fact that a “charge pump” is one of the many known “DC-DC converters” in the art. The purpose of a “charge pump” is to take the DC supply voltage as an input and to provide either a boosted DC voltage or a negative DC voltage as an output. This clearly would be a “DC-DC converter”.

With respect to the second paragraph of page 18, contrary to Appellant’s statement, the rejection is reading element 37 of Doluca et al. as the “current injecting means”. Since the purpose of charge pump 37 of Doluca et al. is to boost the voltage at 19, then it necessarily will inject current thereto.

In the same paragraph, Appellant further argues that “if charge pump 37 was considered the DC-DC converter circuit, then there is no disclosure of the recited current injection circuit”. However, these remarks are not understood because nowhere has Appellant stated which claim is being discussed here. Nowhere is it seen there the charge pump 37 is being interpreted as both the “current injecting circuit” and the “DC-DC converter”. While charge pump 37 is being read as the “DC-DC converter circuit” for claims 1-3, these claims do not recite a “current injecting

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circuit". Further, with respect to claims 4-10, the charge pump 37 is only being interpreted as the "current injection circuit" and not as the "DC-DC converter circuit".

In the remainder of page 18 through the first full paragraph, Appellant discusses elements 31, 35, 39 and 43 as functioning to "compare the fractional voltage of line 19 with V_{ref} and turn on either the charge pump 37 or charge bleeder 45". Appellant then concludes that the elements "do not, however, differentiate variations of an output voltage of the charge pump 37".

Appellant's conclusion is not at all understood. All that is stated in the entire specification concerning elements 12 and 14 is that they are for "differentiating variations in an output voltage of said converter circuit". It would appear that Appellant is given this recited function some unusual and/or improper interpretation. As clearly disclosed in the reference to Doluca et al., and as would be abundantly clear to one skilled in the art of charge pumps, the purpose of elements 31, 33, 39 and 49 is to divide the output voltage at 19 and compare that divided voltage to V_{REF} . This is done for the purpose of determining the relative level of the output voltage at 19. Examiner contends that the operation of determining the relative level of the output voltage would directly correspond to the recited operation of "differentiating variations in an output voltage". If the circuit determines the relative level of the output voltage, it will thus, differentiate variations thereof. Clearly, the purpose elements 12 and 14 of Appellant's Figs 1 and 2 is to enable or disable elements 13 and 15 based on the output voltage OUTPUT. This is precisely the operation provided by the corresponding elements of the circuit to Doluca et al.

With respect the Appellant's remaining remarks, it would appear that this discussion pertains exclusively to claims 7-10. As provided in the rejection and as clearly seen in the reference to Doluca et al., charge pump 37 and charge bleeder 45 are connected in common to


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node 19. Node 19, in turn is connected to a capacitor-plate line of all the capacitors of Fig. 1.

Since the one capacitor (as well as all the others of Fig. 1) relied upon in the rejection is connected to node 19, the claim limitations are met.


For the above reasons, it is believed that the rejections should be sustained.


Respectfully submitted,


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Primary Examiner
Art Unit 2816

January 23, 2004

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